

**REMARKS/ARGUMENTS**

Claims 1-3, 5-10, 12, 15-16 and 18-23 remain in this application. Claims 5, 15, 21 and 22 are withdrawn from consideration. Claims 4, 11, 13-14 and 17 have been cancelled without prejudice. Claims 1, 6, 10, 18 and 23 have been amended to make the claimed inventions more specific.

The Examiner is thanked for the thorough examination of the present application. Applicants have made an amendment to the claims, and assert that the remaining claims are patentable for at least the reasons set forth herein.

**Response to the claim objections:**

Please refer to the specification of the present application. The present invention is generally applied to a communication system which **encodes data as symbol signals** at the transmitter and transmits the symbol signals via a plurality of subchannels. **The symbol signal includes at least two pilot signals**. The subchannels include at least **two pilot subchannels for transmitting a corresponding one of the pilot signals**. The pilot signal is predetermined, and the present invention employs it to estimate and compensate sampling timing offset, thereby preventing the sampling timing offset from impacting signal demodulation at the receiver of the communication system. (Summary of the Invention of pages 2 & 3). Please note that it's **ONE** symbol signal including **TWO** pilot signals (also known to the art as pilot symbols) transmitted via a first and a second subchannels. Therefore, with respect to the disclosure of the specification, applicants have amended claims 1, 10, 18 and 23 and respectfully assert that these amended claims have overcome the indicated informalities.

**Response to the 35 U.S.C. § 103(a) rejections:**

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imamura (U.S. Patent No. 6862262) in view of Nakahara et al. (U.S. Patent No. 7027464, hereafter "Nakahara"). Applicants have carefully read Examination opinion, the cited references Imamura and Nakahara, and found that neither of Imamura, Nakahara and their  
5 combination teaches or suggests the amended claim 1. The amend claim 1 (shown in a clear version) recites:

An apparatus for sampling timing compensation at a receiver of a communication system, wherein each of a first and a second symbol signals comprises two pilot signals transmitted via a first and a second  
10 pilot subchannels respectively, and the first and the second pilot subchannels comprise a first and a second pilot indexes respectively, the apparatus comprising:  
a pilot subchannel estimator for generating a first frequency responses of two of the pilot signals transmitted over the first pilot subchannel and  
15 generating second frequency responses of the other two of the pilot signals transmitted over the second pilot subchannel;  
a timing offset estimator, coupled to the pilot subchannel estimator, for **calculating a timing offset according to** a first difference between the first frequency responses of the first and second symbol signals, a  
20 second difference between the second frequency responses of the first and second symbol signals and **a subtraction between the first and second differences**; and  
a phase rotator, coupled to the timing offset estimator, for performing sampling timing compensation according to a phase rotation  
25 corresponding to the timing offset.

*(Emphasis added)*

It is clearly shown that the claimed invention utilizes not only the first and the second differences calculated according to the first and the second frequency responses

respectively, but also **the subtraction between the first and the second differences** to obtain the timing offset. Imamura, however, at most teaches a phase error calculation circuit 204 for calculating a residual phase error with high estimation accuracy using the residual phase error of each subcarrier calculated by differential detection (*Imamura: Col. 5, lines 59-63*), but is silent on “calculating a timing offset according to **a subtraction between a first and a second differences** which are calculated according to first and second frequency responses respectively”. Although Imamura discloses dividers 305 and 306 and normalization circuits 704, 707 and 1204, each of these circuits just only normalizes **ONE added output** to set its amplitude to 1 (*Imamura: Col. 6, lines 18-21; Col. 8, lines 6-8; Col. 8, lines 16-18; Col. 11, lines 64-66*) but teaches nothing about calculating a timing offset according to **a subtraction between a first and a second differences**. Similarly, Nakahara nowhere discloses the above-mentioned claimed limitations and consequently fails to compensate for the deficiency of Imamura. Therefore, the amended claim 1 is respectfully submitted to be patentable over Imamura in view of Nakahara. Since claims 2-3 are dependent upon claim 1, if claim 1 is found to be allowable, so too should the dependent claims.

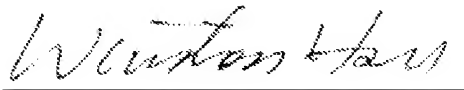
Claims 6, 10-12, 16, 18, 19, 20 and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Imamura in view of Nakahara and Singh et al. (U.S. Patent No. 7139320, hereafter “Singh”). This rejection is respectfully traversed. As explained above, Imamura in view of Nakahara at least fail to disclose “calculating a timing offset according to **a subtraction between a first and a second differences**” as claimed in claims 1, 10, 18 and 23. Singh does not compensate for the deficiencies of Imamura and Nakahara. Therefore, claims 1, 10, 18 and 23 are patentable over Imamura in view of Nakahara and Singh. Since claims 6, 11-12, 16, 19 and 20 dependent upon claims 1, 10, 18 and 23 respectively, if claims 1, 10, 18 and 23 are found to be allowable, so too should the dependent claims.

Claims 7, 8 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Imamura in view of Nakahara, Singh and National (“Application of the ADC1210 CMOS A/D Converter”; National Semiconductor Application Note 245, April 1986). Since claims 7, 8 and 17 are dependent upon claims 1 and 10 respectively and National nowhere teaches or suggest “calculating a timing offset according to **a subtraction between a first and a second differences**”, applicants therefore respectfully assert that claims 7, 8 and 10 are patentable because of at least the same reasons placing claims 1 and 10 allowable.

**Conclusion:**

In view of the above remarks/arguments and amendments set forth above, applicants respectfully request allowance of claims 1-3, 6-10, 12, 16, 18-20 and 23. If the Examiner believes that a telephone interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Sincerely yours,



Date: 07/16/2008

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)